P14VE101 Digital Design

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce NMOS Logic Gates, Simple CMOS Logic Gates and their analysis.*
- *To introduce Sequential System Design Techniques.*
- *To introduce computer-aided minimization procedures such as the CAMP and IISE algorithms.*
- *To introduce PLDs and Advanced FPGA concepts suitable for VLSI circuits*

UNIT – I (12+4)

The Basics **:**Simple NMOS Logic Gates, Simple CMOS Logic Gates, Transfer Curves and Noise margins, Gate Delays and Rise and Fall Times, Transient Response, an RC Approximation to the Transient Response of a CMOS Inverter.

Digital Integrated System Building Blocks: Multiplexors and Decoders, Barrel Shifters, Counters, Digital Adders, Digital Multipliers, Programmable Logic Arrays.

UNIT – II (12+4)

Latches, Flip-Flops And Synchronous System Design**:** CMOS Clocked Latches, Flip-flops, CMOS Flip-flops, Synchronous System Design Techniques, Synchronous System Examples.

UNIT – III (12+4)

Computer Aided Minimization Procedure: CAMP algorithm, Introduction to cube based Algorithms.

Design Of Large Scale Digital Systems: ASM Chart Method. Hardware description language and control sequence method.

UNIT – IV (12+4)

Design using PLAs, PALs, PLDs Programmable Logic Arrays: PLA minimization and PLA folding.

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

Text Books:

1 Ken Martin,*"Digital Integrated Circuit Design"*, Oxford University Press, 2002.
2 N.N.Biswas,*"Logic Design Theory "*, Prentice Hall, 1993
3 Samuel C.Lee and B.S.Sonde, *"Digital Circuits And Logic Design"*, PHI, New Delhi
4 Stephen M.Trimberger *"Field Programmable Gate Array Technology"* Springer International Edn.

Course Learning Outcomes:

After completion of the course the student will be able to

- *Design CMOS Logic Gates with specified noise margin and propagation delay.*
- *Design Combinational Logic blocks.*
- *Learn Synchronous System Design Techniques*
- *Understand PLDs and Xilinx FPGA concepts*

P14VE102 VLSI Technology

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce system design methodology and tools*
- *To introduce the concepts of Scalable CMOS design rules*
- *To introduce the concepts of cell based layout design, interconnect delay modeling, floor planning, and routing.*
- *To introduce different steps involved in fabrication of chip*

UNIT - I (12+4)

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Parasitics – latch up and its prevention, cell concepts.

Design rules – fabrication errors – scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT – II (12+4)

Cell concepts – cell based layout design – Wein berger image array – physical design of logic gates – NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, interconnects delay modeling, floor planning, routing, clock distribution.

UNIT – III (12+4)

Crystal structure, Crystal growth and vapour phase epitaxy. Unit processes for VLSI-Oxidation, Photolithography, diffusion and ion implantation.

UNIT – IV (12+4)

Deposition of metal and dielectric films by vacuum evaporation, sputtering and CVD techniques, Wet chemical and Dry etching techniques.

Text Books:

1 Preas, M. Lorenzatti, "*Physical Design and Automation of VLSI Systems*", The Benjamin – Cummins Publishers, 1998.
2 M. Shoji, "*CMOS Digital Circuit Technology*", Prentice Hall, 1987.
3 John P. Uyemura, "*Introduction to VLSI Circuits and Systems*", John Wiley & sons, Inc.
4 Woyne Wolf, "*Modern VLSI Design (System on Chip)*", Pearson Education, 2002.
5. R. Jacob Baker, Harry W.Li., David E. Boyce, "*CMOS Circuit Design, Layout and Simulation*", IEEE Press, Prentice Hall of India.

Reference Books:

1 S.M. Sze, "*VLSI Technology*" Mc Graw-Hill.
2. "*VLSI Circuit Layout Theory and Design*", Mc Graw-Hill.
3. Randall L. Geiger et.al., "*VLSI Design Technology*", McGraw-Hill Publications.

Course Learning Outcomes:

After completion of the course the student will be able to

- *understand concepts of physical design.*
- *understand CMOS design rules.*
- *understand System level physical design.*
- *understand different steps involved in fabrication*

P14VE103 Discrete Mathematics & Optimization Techniques

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the methods of optimization of both linear and non-linear objectives under a set of constraints.*
- *To introduce the techniques of solving decision making problems and analyze them in a competitive situations to get optimal output.*
- *To introduce the concepts and determination of optimal flow in a transport network and analysis of network scheduling by CPM-PERT with their practical applications.*
- *To introduce the basic concepts of Fuzzy sets, Fuzzy operations, Fuzzy logic and their Engineering applications*

UNIT - I (12+4)

Constrained optimization: Linear programming concepts: Simplex method, Artificial variables method, Duality and Dual simplex method. Integer linear programming: Branch and Bound algorithm, Cutting plane algorithm.

Non-linear Programming concepts: NLPP with equality and inequality constraints. Lagrange's method of multipliers, Kuhn-Tucker Conditions and Penalty function method.

UNIT – II (12+4)

Decision Analysis and Game Theory: Introduction to Decision making Problems. Decision making under uncertainty. Laplace criterion, Max-min criterion, Savage Criterion and Hurwitz criterion. Introduction to Game Theory. Games with Pure strategies. Max-Min and Min- Max Principle. Optimal solution of Two person zero-sum game. Dominance property. Solutions of Mixed strategy games using Graphical and Linear programming methods.

UNIT – III (12+4)

Network Flows: Transport Networks. Flows in a Network and Maximal flows. Max flow- Min cut theorem , Augmenting Path method, Representation of Project Network. Network scheduling by CPM/PERT, Resource analysis in Network scheduling.

UNIT - IV (12+4)

Fuzzy Sets and Fuzzy Logic: Basic concepts of Fuzzy set and examples. Operations on fuzzy sets. Fuzzy complements, Fuzzy intersections, Fuzzy union and their properties. α-cuts and representation fuzzy sets. Generalized fuzzy operations. Complement, t-norms and T- Conorms. Simple theorems on fuzzy operations. Basic concepts of fuzzy logic. Fuzzy propositions and types of Fuzzy propositions. Fuzzy quantifiers. Inferences from conditional fuzzy propositions, qualified propositions and quantified propositions.

Text Books:

1 Kandell, J.L Mott and Backer, "*Discrete Mathematics*", Prentice Hall of India, 2nd Edn.,, 1986.

2 George J.Kilr, Boyuan, "*Fuzzy Sets and Fuzzy logic*", Prentice Hall of India, 2003.

3 Kanti Swaroop, P.K. Gupta, ManMohan, "*Operations Research*", S.Chand Publications, 11th Edn., 2010.

4 H.A. Taha, "*Operations Research an Introduction*", Prentice Hall of India, 6th Edn., 2006

Reference Books:

1 J.C. Panth, "*Introduction to optimization and operation research*", Jain Brothers, 7th Edn., 2006.

2. S.S.Rao, "*Engineering Optimization, Theory and Practice*", New Age International (P) Ltd Publishers, 3rd Edn. 2013

Course Learning Outcomes:

After completion of the course the student will be able to

- *Solve any type of LPP and discuss the nature of the solution.*
- *Solve a class of non-linear programming problems with different types of constraints.*
- *Identify the importance of decision making systems and find an optimal solution of the problem given different types of nature of states.*
- *Analyze different strategies of a Game between two objects under conflicting situations.*
- *Develop an algorithm for solving problems of Game theory.*
- *Find a maximal flow of commodities in a transport network using different methods.*
- *Discuss different network based methods designed to assist in the planning, scheduling and control of projects.*
- *Identify the differences between Crisp sets and Fuzzy sets and the related properties.*
- *Differentiate between Classical systems and Fuzzy systems in order to solve the problems based on Fuzzy logic*

P14VE104 Embedded System Design

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce various hardware and software embedded structures in real time applications*
- *To introduce the basic the design concepts of embedded systems*
- *To introduce the Communication protocol concepts of embedded systems*
- *To introduce methods Inter processor communication*

UNIT – I (12+4)

Introduction to Embedded Systems:
Characteristics, Different Types of Embedded Systems, Components of Embedded System, Hardware Architecture, Processor, Peripheral Devices, Embedded Software Architecture, Need of Real Time Operating Systems and Different Application Areas.
Processor and Memory Selection:
Different Types of Processor Technologies, Processor Selection for an Embedded System,Different Types of Memory Devices, Memory Selection for an Embedded System.

UNIT – II (12+4)

Communication Interfacing: Communication protocol concepts, Microprocessor interfacing: I/O addressing, Port and Bus based, I/O, Memory Mapped I/O, Standard I/O interrupts, Direct memory access, Serial Communication Protocols I2C, CAN, Parallel Communication Protocols PCI bus, PCI-X and Wireless protocol IrDA, blue tooth.
Device Drivers and Interrupts Servicing Mechanism:
Different types of Interrupts, Interrupt Servicing Mechanism, Device Servicing using ISR, Device Drivers, Parallel Port and Serial Port Device Drivers and Device driver Programming

UNIT – III (12+4)

Software Engineering Practices in the Embedded Software Development Process: Software Development Life Cycle and its Models, Software Analysis, Software Design, Software Implementation, Software Testing , Validating and Debugging, Real Time Programming Issues During the Software
Development Process, Software Project Management, Software Maintenance , Unified Modeling Language(UML)

UNIT – IV (12+4)

Programming models for Single and Multiprocessor Systems: DFG, CDFG,FSM, Petri nets, SDFG, HSDF, APEG and MTG
Inter-Process Communication and Synchronization of Processes, Tasks And Threads: Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Inter Process Communication

Text Books:

1 Raj Kamal, "*Embedded Systems*", Tata McGraw Hill, 2003.
2 Frankvahid/Tony Givargis, "*Embedded System Design- A Unified Hardware/software Introduction*"
3 Jane W.S. LIU., "*Real Time Systems*", Pearson Education, Asia, 2001.
4 Dream Tech Software Team, "*Programming Embedded Systems*", John Wiley Pub, 2004.

Reference Books:

1 C.M. Krishna and G. Shin, "*Real Time Systems*" McGraw-Hill International Edn., 1997
2. Daniel W.Lewis, "*Fundamentals of Embedded Software-where C and Assembly meet*", Pearson Education, 2002

Course Learning Outcomes:

After completion of the course the student will be able to

- *Design a embedded system for real time applications*
- *Handle interrupts in embedded system development*
- *Understand Software Engineering Practices in the Embedded Software Development Process*
- *Understand inter processor communication and synchronization*

P14VE105 A Hardware Description Languages

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce Dataflow & structural modeling programs using VHDL.*
- *To introduce Sequential modeling using VHDL.*
- *To introduce design styles used in HDLs.*
- *To introduce the design using Verilog HDL*

UNIT - I (12+4)

Introduction: About VHDL, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading

UNIT – II (12+4)

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits

UNIT – III (12+4)

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to One-Hot

UNIT - IV (12+4)

Introduction to Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling. Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior

Text Books:

1 Volnei A. Pedroni, *"Circuit Design and Simulation with VHDL"*, 2nd Edn., MIT Press, 2010.
2 Kenneth S Kundert, Olaf Zinke, *"Designers Guide to Verilog AMS"*, Springer, 2004.
3 Samir palnitkar, *"Verilog HDL"*,Pearson Education Asia ,New Delhi,2001

Course Learning Outcomes:

After completion of the course the student will be able to

- *Write Dataflow & structural modeling programs using VHDL.*
- *Differentiate Concurrent & Sequential Design.*
- *Design State Machines with different styles.*
- *Learn Concepts of Verilog HDL*

P14VE105 B Semiconductor Device Modeling

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the concepts of energy band in solids and design of bipolar devices.*
- *To introduce performance characteristics of CMOS devices.*
- *To introduce different MOSFET DC Models.*
- *To introduce Optoelectronic Devices and Spice Models for Semiconductor devices*

UNIT – I (12+4)

Basic Device Physics :Energy bands in solids , p-n Junctions, MOS Capacitors, Metal-Silicon Effects, MOSFET Devices Design: Long Channel MOSFET, Short-Channel MOSFETS, MOSFET Scaling, Threshold Voltage.

Bipolar Devices Design: npn & pnp Transistors, Ideal Current-Voltage Characteristics, Bipolar Device Models for Circuit and Time-Dependent Analyses, Modern Bipolar Transistor Structures, Figures of Merit of a Bipolar Transistors, Digital Bipolar Circuits

UNIT – II (12+4)

CMOS Performance characteristics: Basic CMOS Circuit Elements, Parasitic Elements, Sensitivity of CMOS delay to device parameters, Performance characteristics of Advanced CMOS Devices.

UNIT – III (12+4)

MOSFET DC Model: Drain Current Calculations, Pao-Sah Model, Charge Sheet Model, Piece-Wise Drain Current Model for Enhancement Devices.

UNIT – IV (12+4)

Optoelectronics Devices: Light emitting diodes, Lasers, Photoconductors, Junction Photodiodes, Avalanche Photodiodes, Solar Cells, SPICE Models for Semiconductor Devices: MOSFET Level 1, Level 2 and level 3 model, Model parameters; SPICE models of p-n diode and BJT.

Text Books:

1 Ben G Streetman, "*Solid State Electronic Devices*", 6th Edn., Pearson Prentice-Hall, 2009.
2 B. G. Streetman and S. Banerjee, "*Solid State Electronic Devices*", 6th Edn, PHI, 2011.
3 P. Bhattacharya, "*Semiconductor Optoelectronics Devices*", 2nd Edn., PHI, 2009.

Reference Books:

1 G. Massobrio and P. Antognetti, "*Semiconductor Device Modeling with SPICE*", 2nd Edn., TMH, 2010.
2 C. C. Hu, "*Modern Semiconductor Devices for Integrated Circuits*", Pearson Education, 2010.
3 S. M. Sze and K. K. Ng, "*Physics of Semiconductor Devices*", 3rd Edn., Wiley India, 2010.

Course Learning Outcomes:

After completion of the course students will be able to

- *understand bipolar device models and apply SPICE models to Semiconductor Devices.*
- *understand CMOS Performance characteristics .*
- *analyze MOSFET DC models*
- *describe the basic operation of Optoelectronics Devices*

P14VE105C Scripting Languages for VLSI Design Automation

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the basics of various scripting languages such as PERL, CGI, VB Script, Java Script .*
- *To introduce the programs based on PERL.*
- *To introduce the concepts of inter processes communication threads .*
- *To introduce programming concepts in PERL, VB Script and JAVA script*

UNIT – I (12+4)

Overview of Scripting Languages-PERL, CGI, VB Script, Java Script.

UNIT – II (12+4)

PERL:
Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables

UNIT – III (12+4)

Inter process Communication Threads, Compilation & Line Interfacing.

UNIT – IV (12+4)

Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL.
Other Languages:
Broad Details of CGI, VB Script, Java Script with Programming Examples.

Text Books:

1 Randal L, Schwartz Tom Phoenix, "*Learning PERL*"
2 Larry Wall, Tom Christiansen, John Orwant, "*Programming PERL*".

Course Learning Outcomes:

After completion of the course students will be able to

- *Learn the basics of various scripting languages..*
- *Understand the programs based on PERL.*
- *Get familiarized with the inter process communication threads .*
- *learn programming skills in PERL, VB Script and JAVA script*

P14VE105D Computer Aided Circuit Simulation

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To formulate equations and solve nonlinear networks*
- *To introduce special classes of multistep methods for the solution of electrical networks.*
- *To introduce general purpose circuit simulators .*
- *To introduce physical or empirical models of semiconductor parameters in small signal analysis*

UNIT – I (12+4)

Formulation of network equations: Nodal, mesh, modified nodal and hybrid analysis equations.; Sparse matrix techniques; Solution of nonlinear networks through Newton-Raphson technique.; Multistep methods: convergence and stability;

UNIT – II (12+4)

Special classes of multistep methods: Adams-bashforth, Adams-Moulton and Gear's methods; Solution of stiff systems of equations; Adaptation of multistep methods to the solution of electrical networks;

UNIT – III (12+4)

General purpose circuit simulators.; Review of semiconductor equations (Poisson, continuity, drift-diffusion, trap rate). Finite difference formulation of these equations in 1D and 2D. Grid generation.;

UNIT – IV (12+4)

Physical/empirical models of semiconductor parameters (mobility, lifetime, band gap, etc.).; Computation of characteristics of simple devices (p-n junction, MOS capacitor, MOSFET, etc.); Small-signal analysis.

Text Books:

1 L.O.Chua and P.M.Lin, "*Computer Aided Analysis and Electronic Circuits*", PHI

2 S. Selberherr, "*Analysis and Simulation of Semiconductor Devices*", Springer-Verlag, 1984.

3 N.J. McCalla, "*Fundamentals of Computer Aided Circuit Simulation*", Kluwer Academic Publishers, 1988

Course Learning Outcomes:

After completion of the course students will be able to

- *Solve nonlinear networks*
- *apply multistep methods and solve electrical networks.*
- *Apply general purpose circuit simulators.*
- *Use physical and empirical models in computation of semiconductor device characteristics.*

P14VE106A Advanced Microprocessor and Microcontroller

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To expose the students to the fundamentals of microprocessor architecture.*
- *To introduce the advanced features in microprocessors and microcontrollers.*
- *To enable the students to understand various microcontroller architectures*

UNIT – I (12+4)

16 Bit Microntrollers: 8096/196 family microcontrollers Architecture, instruction set programming, interrupts, timers, serial communication programming

UNIT – II (12+4)

MC68HC11 family microcontrollers: Architecture, interrupts, timers.

Instruction set addressing modes – operating modes programming - Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.
PIC MICROCONTROLLER CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

UNIT – III (12+4)

Interfacing Methods: Switch, key board, display (LED, LCD), printer, motor, memory ADC, DAC I/o interfacing methods, C programming basics for Microcontrollers

UNIT – IV (12+4)

Arcon RISC Machine – Architectural Inheritance – Core & Architectures – Registers – Pipeline – Interrupts – ARM organization – ARM processor family – Co-processors – ARM instruction set- Thumb Instruction set – Instruction cycle timings – The ARM Programmers model – ARM Development tools – ARM Assembly Language Programming – C programming – Optimizing ARM Assembly Code – Optimized Primitives.

Text Books:

1 M.A.Mazadi & J.G.Mazidi, " *The 8051 Micro controller & Embedded Systems*", Pearson Education, Asia (2000)

2 Raj Kamal, "*Microcontrollers Architecture, Programming, Interfacing, system Design*", Pearson Edcuation. Asia

3 S.Fuber, "*ARM system on-Chip Architecture*", 2nd Edn., Addison Wisley, Great Briton-2000 John B.Peatman, " *Designing with PIC Micro controllers*", Pearson Education.

4 Ajay V.Deshmukh, " *Microcontrollers theory and applications",* Mc.Graw Hill

Course Learning Outcomes:

After completion of the course the student will be able to

- *The student will be able to work with suitable microprocessor / microcontroller for a specific real world application*

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P14VE106B Data Communication Computer Networks

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce transmission media protocols & routing*
- *To introduce Access techniques, IEEE 802 standards, switched and Fast Ethernet.*
- *To introduce Network Protocols & Inter-networking*
- *To introduce the concepts of Quality of service , network security and management.*

UNIT – I (12+4)

Introduction to Network components, switching technologies, topologies, transmission media, protocols & routing.

WAN, NAN, LAN. Queuing theory models and applications computer networks, Data communication concepts – asynchronous & synchronous transmission, error correction codes & detectors.

UNIT – II (12+4)

Transmission Protocols**:**

STOP – START, BSC, SDLC, HDLC, Retransmission techniques. LAN – components, Topologies, Access techniques, IEEE 802 standards, switched and Fast Ethernet, FDDI & SONET.

UNIT – III (12+4)

Network Protocols – concepts, layers, Architecture, OSI model – X.25, TCP/IP layers – addressing & routing in an Internet, Major application layers, near services: a mail, www., F.T.P., Telnet. Backbone networks / Inter-networking – Devices: Switches, Hubs, Bridges, routers, gateways and choice for implementation.

UNIT - IV (12+4)

Broad band Networks – ISDN, ATM, Protocol. Quality of service & Traffic management concepts, VSAT Networks. Brief ideas on network security and management.

Text Books:

1 Black. U, "*Computer Networks, Protocols, Standards and Interfaces*", PHI 1997
2 Tahenbanm S.A., "*Computer Networks*", PHI, 1996.
3 Stalling W., "*High Speed Networks: TCP/IP and ATM Design principles*", PHI, 1998.

Reference Books:

1 Shanmugam A, Rajeev S, "*Computer Communication Networks*", ISTE learning material center, 2001.
2. Stalling. W, "*ISDN and Broadband ISDN with Frame Relay and ATM*", 3rd Edn., PHI, 1998.
3. Charles.P.Pleegar, "*Security in Computing*", PHI

Course Learning Outcomes:

After completion of the course students will be able to

- *understand protocols & routing ,switching technologies, topologies, transmission media and its applications.*
- *understand IEEE 802 standards, Fast Ethernet, FDDI & SONET.*
- *understand OSI model – X.25, TCP/IP layers in an Internet.*
- *understand Quality of service and ideas on network security and management*

P14VE106C Data Structures & Algorithm Analysis

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce concepts of linked lists, stacks and queues*
- *To introduce sorting techniques.*
- *To introduce searching techniques and its applications.*
- *To introduce the techniques for designing algorithms*

UNIT - I (12+4)

Introduction to DS:
Lists, Stacks and queues, abstract data types ,the list ADT-the stack ADT, the queue ADT
Trees: Preliminaries, binary trees , the search tree ADT, binary search trees , AVL trees, splay trees, B- Trees.

UNIT – II (12+4)

Sorting
Internal sorting, preliminaries, insertion sort, a lower bound for simple sorting Algorithms, Shell sort, heap sort, merge sort, quick sort, bucket sort,, external sorting.

UNIT – III (12+4)

Graph algorithms:
Definitions, Topological sort, Shortest path Algorithms, Minimum Spanning Tree, Applications of depth- first search: unidirected graphs, bio-connectivity, directed graphs, finding strong components.
Hashing: Hash function, separate chaining, open addressing, rehashing, extendable hashing.

UNIT – IV (12+4)

Algorithm design techniques:
Greedy algorithms, divide and conquer, dynamic programming
Introduction to NP-completeness:
Easy versus hard, the class NP,NP-complete problems.

Text Books:

1 Mark Allenweiss, "*Data Structures and Algorithm Analysis in C++*", 2nd Edn, Pearson Education,2004.

2 Ellis Horowitz, Sartaj Sahni and Sanguthevar Rajasekaran, "*Computer Algorthims/C++",* Universities Press (India) Private Limited, 2nd Edn., 2007.

Reference Books:

1 A. V. Aho, J. E. Hopcroft, and J. D. Ullman, "*Data Structures and Algorithms",* 1st Edn., Pearson Education, 2003.

2 R. F. Gilberg and B. A. Forouzan, "*Data Structures*", 2nd Edn.,Thomson India Edition, 2005.

3. Robert L Kruse, Bruce P Leung and Clovin L Tondo, "*Data Structures and Program Design in C"*, Pearson Education, 2004.

Course Learning Outcomes:

After completion of the course students will be able to

- *write programs for linked lists, stacks and queues*
- *analyze and compare sorting techniques*
- *Apply searching techniques in data analysis*
- *understand the algorithm development methods*

P14VE106D Digital Filter Design

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the concepts of the basic Multirate techniques like interpolation, decimation of DSP.*
- *To learn stationary random process, Rational power spectra Auto-correlation sequence.*
- *To introduce the Optimum reflection coefficients for the Lattice forward and backward Predictors.*
- *To introduce the Properties of Linear Prediction error filters, orthogonality principle in Linear Mean-Square Estimation*

UNIT – I (12+4)

Multirate Digital Signal Processing:
Introduction – Decimation by integer factor. Interpolation by an integer factor. Sampling rate conversion by non-integer factors. Multistage approach to sampling rate conversion. Design of practical sampling-rate converters. Software implementation of interpolators and decimators. Sample rate conversion using polyphase filter structure. Examples of applications of multirate DSP.

UNIT – II (12+4)

Linear Prediction and Optimum Linear Filters:
Representation of a stationary random process. Rational power spectra-AR, MA & ARMA processes. Relationship between the filter parameters and Auto-correlation sequence. Forward and Backward linear prediction

UNIT – III (12+4)

Optimum reflection coefficients for the Lattice forward and backward predictors. AR process and linear prediction. Solution of Normal equations. Levinson-Durbin algorithm. The Schur algorithm. Pipelined architecture for implementing the Schur algorithm

UNIT - IV (12+4)

Properties of Linear Prediction error filters. AR Lattice and ARMA Lattice-Ladder filters. Wiener filters for filtering and prediction. Orthogonality principle in Linear Mean-Square Estimation.

Text Books:

1 E.C. Ifeachor et.al., "*Digital Signal Processing*" Pearson Education Asia Publication, 2nd Edn. (2002)

2 John G.Proakis, C.M. Radar et.al., "*Algorithms for Statistical Signal Processing*" by Pearson Education Asia Publication, 2nd Edn. (2002).

Reference Books:

1 Dimitris G. Manolakis et.al., *"Statistical & Adaptive Signal Processing"*, Mc. GrawHill International Edn. (2000).

Course Learning Outcomes:

After completion of the course students will be able to

- *understand the practical sampling-rate converters interpolators and decimators.*
- *Identify the processes characterstics from the transfer function*
- *Use different algorithms such as Levinson-Durbin algorithm, Schur algorithm*
- *learn various Properties of Linear Prediction error filters*

P14VE107 VLSI Technology Laboratory

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
0	0	3	2

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce Layouts of basic devices and algorithms*
- *To introduce placing and routing algorithms*
- *To introduce concepts of interconnect delay modelling*
- *To introduce automatic layout tools and design rule checkers*

List of Experiments:

1. Layout of Basic Devices
2. Partitioning Algorithms
3. Place and Route Algorithms
4. Floor Planning and Pin Assignment
5. Routing, DRC & Automatic Layout Tools
6. Clock distribution
7. Interconnect Delay modeling
8. Modeling and Extraction of circuit parameters from Physical layout.
9. Mini Project – 2

Note: As a part of this Laboratory course students has to takeup TWO mini projects .

Report is to be submitted

Course Learning Outcomes:

After completion of the course students will be able to

- *To learn Layouts of basic devices and algorithms*
- *To understand placing and routing algorithms*
- *To learn concepts of interconnect delay modelling*
- *To understand concepts of automatic layout tools and design rule checkers*

P14VE108 Digital Design Laboratory

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
0	0	3	2

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce modeling styles used in Verilog*
- *To introduce Sequential System Design using Verilog.*
- *To introduce implementation of circuits using Bit-wise, logical and reduction operators.*
- *To introduce implementation of Finite State Machines and Sequence Detectors*

List of Experiments: (Using Verilog)

Simulation of

1. Ripple Carry Adder using Gate Level modeling.
2. Carry Look-Ahead Adder using Data Flow modeling.
3. Ripple Counter in Data Flow modeling.
4. A Magnitude Comparator in data flow modeling.
5. Traffic Signal Controller in behavioral modeling.
6. 8 function ALU that takes 4-bit inputs in behavioral modeling.
7. Finite State Machines realization.
8. Sequence Detectors.
9. Mini-projects-2

Note: As a part of this Laboratory course students has to takeup TWO mini projects .

Report is to be submitted

Course Learning Outcomes:

After completion of the course students will be able to

- *design Logic Gates using HDLs.*
- *design Combinational Logic blocks.*
- *design Synchronous System Design using HDLs.*
- *design state machines.*

P14VE109 Seminar

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
-	-	-	2

Examination Scheme:

Continuous Internal Evaluation:	100 marks
End Semester Exam :	-----

1 There shall be only Continuous Internal Evaluation (CIE) for Seminar, which includes Report Submission & Presentation

2 A teacher will be allotted to a student for guiding in
(i) selection of topic
(ii) report writing
(iii) Presentation (PPT) before the DPGRC on a pre notified date

P14VE201 Mixed Signal Design

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the concepts of Analog design techniques.*
- *To introduce the design techniques for differential amplifiers and operational amplifiers.*
- *To introduce concepts of MOS OPAMPS with cascade.*
- *To introduce concepts of data converters.*

UNIT – I (12+4)

Introduction to analog design , need for analog design, analog IC design flow. Brief Review of Small Signal and Large Signal Model of BJTs and MOSFETs. Current Mirrors and Single Stage Amplifiers–Simple CMOS current sinks and sources, MOS current mirror, Common Source Amplifier, Source follower, common gate amplifier, cascode amplifiers. Source degenerated current mirrors. High output impedance – current mirrors, cascode stage Wilson current mirror. Bipolar current mirrors – Bipolar gain stages. widlar current mirror.

UNIT – II (12+4)

Differential amplifiers – single ended and Differential operation, Basic Differential pair , common mode response and Differential pairs with MOS loads.
Operational amplifiers – General considerations, one stage OPAMPS, two stage OPAMPS. Gain Boosting , comparison, common mode feedback , Input range limitations, slew rate and power supply rejections

UNIT – III ((12+4)

Two stage MOS OP-AMP with cascodes. MOS Telescopic cascode OPAMP . MOS Folded cascode OP-AMP. Current feedback OPAMPS. Stability and frequency compensation of OP-AMPs , Gain margin and Phase margin OPAMPS

UNIT – IV (12+4)

Data converter fundamentals: Ideal D/A converter, Ideal A/D converters, Quantization noise , signed codes, performance limitations.

D/A Converters: - decoder based converter, binary – Scaled Converters, Thermometer code converter, hybrid converters.

A/D Converters: Integrated converters - successive approximation, Cyclic A/D Converters, Flash or parallel converters, Two step A/D converters, interpolating A/D converters, F A/D converters.

Text Books:

1 R.Gregorian, Temes,"*Analog MOS integrated circuits for Signal processing*".
2 R.Gregorian,"*Introduction to CMOS opamps and comparators*".
3 D.Johns, K.Martin, "*Analog integrated circuit design*".
4 Mohammed Ismail, Terrifiez, "*Analog VLSI*", McGraw-Hill, 1994.
5. B.Razavi,"*Monolithic Phase-locked loops and clock recovery circuits*".
6. Behzad Razavi, "*Design of Analog CMOS Integrated Circuit Design*", Tata McGraw Hill

Course Learning Outcomes:

After completion of the course students will be able to

- *understand the significance of analog design and its applications*
- *design and analyze differential amplifiers and operational amplifiers*
- *acquire the ability design cascade amplifiers.*
- *understand the fundamentals of data converters.*

P14VE202 RTOS for Embedded Systems

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the Unix Operating systems and process management*
- *To introduce the POSIX OS and IEEE standard 1003.13.*
- *To introduce the Real time Operating System concepts and kernel structure.*
- *To introduce the LINUX: Kernel real time extensions, scheduling threads, root file system and VX works OS.*

UNIT – I (12+4)

Brief review of Unix operating systems (Unix kernel-file system, concept of- process, concurrent execution and interrupt. process management–fork and execution. Programming with system calls, process scheduling .shell programming and filters).

Portable operating system interface (POSIX)-IEEE standard 1003.13 & POSIX real time profile .POSIX versus traditional unix signals overheads and timing predictability.

UNIT – II (12+4)

RTOS:
Real time systems concepts, open system architecture and issue .hard and soft real time system. RTOS kernel and issue in multi tasking-task assignment scheduling, inter task communication and synchronization. classical uniprocessor algorithms, scheduling, processer utilization. Application programming interface(API), RTAPI-capabilities

UNIT – III (12+4)

Commercial Real Time Operating Systems :
Micro C /OS-Real time Kernel &KERNEL structured and its working .application to embedded systems.(LYNOX)-Micro Kernel & Kernel plug-ins (KPIs) for i/o support self hosted systems for embedded application).

PSOS systems-PSOS+(a Real time Kernel for a single micro processor application) system Architecture and Modularity, feature: task management and scheduling, time management is i/o systems , driver interface environment –integrated development tools and host based debugging tools, brief ideas on PSOS+(a Microprocessor kernel & features).POSIX compliance, networking programming.

UNIT – IV (12+4)

LINUX: Kernel real time extensions, scheduling threads, root file system.
VX Works—POSIX Real Time Extensions, timeout features and wind semaphores and memory management – virtual to physical address mapping. Debugging tools and cross development environment. Comparison of commercial RTOS – LYNXOS, PSOS, QNX/Neutrino VLTS, VX Works, RTOS for embedded Applications.

Text Books:

1 Jane W.S.LIU., "*Real Time Systems*". Pearson Education, Asia, 2001.

2 Betchof, D.R., *"Programming with POSIX threads"* Addison–Wesley Longman, 1997

3 Motorola, "*PSOS +TM/68 Real Time Executive*", Users Manual Motorola, Inc.

4 Wind River Systems, "*VX Works Programmers Guide*", Wind Revir Systems Inc, 1997.

Reference Books:

1 "*Computer Architecture and Parallel Processing*", McGraw-Hill International Edn

2. Gallmeister ,B.O., *"POSIX.4: Programming for Real World"*, G.Reilly & Associates, Inc.,1995.

3 C.M.Krishna, G.Shin,"*Real Time Systems"*McGraw-Hill International Edn. 1997

Course Learning Outcomes:

After completion of the course students will be able to

- *understand the basic differences between different Operating systems.*
- *learn the POSIX OS and IEEE standard 1003.13.*
- *understand the Real time Operating System concepts and kernel structure.*
- *understand the concept of LINUX OS,VX works OS and other RTOS for embedded systems.*

P14VE203 Low Power VLSI Design

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce Physics of power dissipation in CMOS*
- *To introduce low voltage CMOS circuit design styles.*
- *To introduce concepts of Low power architectures.*
- *To introduce Software design for low power*

UNIT – I (12+4)

Introduction and need of low power design sources of power dissipation and design strategies for low power. Physics of power dissipation in CMOS - low power VLSI design limits. Power estimation at circuit level – modeling of signals, signal probability calculations, statistical techniques, input vector compaction, circuit reliability. Synthesis for low power – behavior level transforms, logic and circuit level optimization.

UNIT – II (12+4)

Design styles and testing – low voltage CMOS circuit design styles, leakage current in deep submission transitions and design issues, minimization of short channel effects (SCE) and hot carrier effects. Testing of deep sub micron ICs with elevated intrinsic leakage.

UNIT – III (12+4)

Low power architectures – MOS static RAM cells, banked organization SRAMS, reducing voltage swing on bit lines, write lines, driver circuits and sense amplifier circuits. Energy computing and recovery techniques – energy dissipation using an RC model, energy recovery circuit design, design with partially reversible logic and supply clock generation.

UNIT – IV (12+4)

Software design for low power - dedicated hardware Vs software implementation, power dissipation, estimation and optimization. Automated power code generation and co design for low power.

Text Books:

1 Kaushik Roy, Sharad Prasad, "*Low Power CMOS VLSI Circuit Design*", John Wiley & Sons, 2000.
2 A.P. Chandrakasan, R.W. Broderson, "*Low Power design*", IEEE Press, 1998.
3 J.B. Kuo, J.H. Juo, "*Low Voltage VLSI Circuits*", John Wiley & Sons.

Course Learning Outcomes:

After completion of the course students will be able to

- *know sources of power dissipation and design strategies for low power.*
- *analyze Design styles and testing.*
- *design MOS static RAM cells, banked organization SRAMS.*
- *know hardware & software co design for low power.*

P14VE204 Hardware & Software Co-Design

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the basic concepts of hardware software co design.*
- *To introduce the Software and hardware Implementation of Data Flow.*
- *To understand the Analysis of Control Flow and Data Flow.*
- *To learn the concepts of System On Chip*

UNIT – I (12+4)

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design, Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

UNIT – II (12+4)

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.

UNIT – III (12+4)

Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph4.4 Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph. Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor

UNIT – IV (12+4)

System on Chip: The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co- Processor.

Text Books:

1 Patrick Schaumont, *"A Practical Introduction to Hardware/Software Co-design"* Springer, 2010

2 Ralf Niemann, *"Hardware/Software Co-Design for Data flow Dominated Embedded Systems"*, Springer, 1998.

Course Learning Outcomes:

After completion of the course students will be able to

- *understand the Nature of Hardware and Software co design*
- *implement the Software and hardware for Data Flow.*
- *understand the Analysis of Control Flow and Data Flow, Finite State Machine With Datapath.*
- *design the System On Chip Architecture and various Processors*

P14VE205A ASIC Design

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce ASIC's Design Flow & ASIC Library Design*
- *To introduce architectures of Actel & Xilinx ASICs.*
- *To introduce concepts of Programmable ASIC Design Software*
- *To introduce algorithms for ASICS/ SoCs as case studies*

UNIT – I (12+4)

Introduction, Types of ASIC's Design Flow, CMOS Logic. ASIC Library Design, Transistor Parasitic capacitance, slew rate, Library cell design Architecture. Programmable ASICs, The Antifuse Metal Antifuse, Static RAM, EPROM and EEPROM Technology, Practical Issues.

UNIT – II (12+4)

Programmable ASIC Logic Cells, Actel,Xilinx LCA., XC3000 CLB, XC4000 Logic Block, XC5200 Logic Block, Xilinx CLB Analysis,. Logic Expanders.. Programmable ASIC I/O Cells,Totem-Pole Output, Mixed-Voltage Systems, Metastability, Xilinx I/O Block. Boundary Scan.

UNIT – III (12+4)

Programmable ASIC Interconnect and Programmable ASIC Design Software.Actel ACT, RC Delay in Antifuse Connections, Xilinx EPLD Logic Synthesis, FPGA Synthesis, Third-party Software. low level design entry, logic synthesis, simulation,

UNIT – IV (12+4)

High performance algorithms for ASICS/ SoCs as case studies –Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance filters using delta-sigma modulators, USB controllers, OMAP.

Text Books:

1 Michel John Sebastian Smith, *"Application Specific Integrated Circuits"*, Addison Wesley Professional, 2008.

2 Himanshu Bhatnagar, *"Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler"*, 2nd Edn., Kluwer Academic, 2001.

Reference Books:

1 H.Gerez, *"Algorithms for VLSI Design Automation"*, John Wiley, 1999

2. Hoi-Jun Yoo, Kangmin Leeand Jun Kyong Kim, *"Low-Power NoC for High-Performance SoC Design"*, CRC Press, 2008

3. SudeepPasricha and NikilDutt, *"On-Chip Communication Architectures System on Chip Interconnect"*, Elsveir, 2008

Course Learning Outcomes:

After completion of the course students will be able to

- *know Architecture of Programmable ASICs.*
- *analyze Programmable ASIC Logic Cells.*
- *understand Programmable ASIC Interconnect .*
- *write algorithms for ASICS/ SoCs as case studies*

P14VE205B VLSI Signal Processing

Class: M.Tech. I Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce techniques for altering the existing DSP structures to suit VLSI implementations.*
- *To introduce efficient design of DSP architectures suitable for VLSI*

UNIT - I (12+4)

Introduction To Dsp Systems, Pipelining And Parallel Processing Of Fir Filters

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm,Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT – II (12+4)

Retiming, Algorithmic Strength Reduction

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT – III (12+4)

Fast Convolution, Pipelining And Parallel Processing of Iir Filters

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT – IV (12+4)

Bit-Level Arithmetic Architectures

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

Text Books:

1 Keshab K. Parhi, " *VLSI Digital Signal Processing Systems, Design and implementation* ", Wiley, Interscience, 2007.

2 U. Meyer – Baese, " *Digital Signal Processing with Field Programmable Gate Arrays*", Springer, Second Edition, 2004

Course Learning Outcomes:

After completion of the course the student will be able to

- *Ability to modify the existing or new DSP architectures suitable for VLSI*

P14VE205 C Microchip Fabrication Techniques

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce International Technology Roadmap for Semiconductors*
- *To introduce Semiconductor Materials and Process Chemicals*
- *To introduce fabrication of wafers*
- *To introduce contamination control process yield*

UNIT – I (12+4)

Semiconductor Industry - Birth of Industry, Evolution

UNIT – II (12+4)

Semiconductor Materials and Process Chemicals, Semiconductor Material Preparation, Crystal grown.

UNIT – III (12+4)

Manufacturing Wafers: Wafer preparation. Overview of Wafer Fabrication.

UNIT – IV (12+4)

Contamination Control:- Contaminants, Contamination, caused problems, Contaminant Sources, Clean Air Strategies, Clean Room Work Station Strategy and Clean Room Construction.

Text Books:

1 "*Microchip Fab Techniques*" by Peter Vanzant(4M Edition)

Course Learning Outcomes:

After completion of the course students will be able to

- *understand International Technology Roadmap for Semiconductors*
- *understand Semiconductor Materials and how Process Chemicals.*
- *understand fabrication process of wafers.*
- *understand control process yield*

P14VE205D Design for Testability

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the basic concepts of Design for Testabilty and modeling techniques*
- *To familiarize the testing for single stuck at faults , ATG pattern generation.*
- *To introduce the various DFT approaches for digital design.*
- *To learn the concepts of Built in Self test(BIST) and Memory BIST.*

UNIT - I (12+4)

Introduction to Test and Design for Testability (DFT) Fundamentals

Modeling:

Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation. Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT – II (12+4)

Testing for single stuck at faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT – III (12+4)

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – IV (12+4)

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST):

Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Text Books:

1 Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, "*Digital Systems Testing and Testable Design*", Jaico Publishing House, 2001.

2 Alfred Crouch, "*Design for Test for Digital ICs & Embedded Core Systems*", Prentice Hall.

Course Learning Outcomes:

After completion of the course students will be able to

- *understand the need of Testing and Testabilty*
- *learn different fault models and various test pattern generation methods.*
- *design the various DFT approaches for digital design and compression*
- *learn the different approaches for Built in Self test(BIST) and Memory BIST*

P14VE206A Industrial Applications of Embedded Microcontrollers

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce various process industrial applications*
- *To expose different interfacing technologies*
- *To Learn automobile industry applications*
- *To introduce wireless communication applications*

UNIT – I (12+4)

Process Industrial applications robot ARM programming tools Optical rotary shaft, encoder, LVDT interfacing, special temperature load cell, ILC interface, software protocol, communication home automation & control/ applications

UNIT – II (12+4)

Zigbee interface, Ethernet interface, LED interface, LCD interface GLID interface

UNIT – III (12+4)

Automobile industry applications motor control interface, CAN interface

UNIT – IV (12+4)

Wireless communication applications wireless networking and implementation of 802.11 with microcontroller

Text Books:

1 Parab J, Shine S. A, *"Practical Aspects of Embedded System Design using Microcontrollers"*, Springer 2008

2 Rajiv Kapadia ,*"8051 Microcontroller & Embedded Systems "*

Course Learning Outcomes:

After completion of the course the student will be able to

- *Understand process industrial applications*
- *Understand various interface technologies*
- *Understand automobile industry applications*
- *Understand wireless communication applications*

P14VE206B Advanced Computer Systems Architecture

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To learn Multi processor systems and their bus communication*
- *To learn Principles of pipelining and parallelism*
- *To learn cache coherence, message passing mechanisms in Multi processors systems*
- *To learn Multi threading environments*

UNIT – I (12+4)

Introduction to Parallel Processing: Evolution of computer systems, Parallelism in Uniprocessor systems, Parallel Computer Structures. Architectural classification schemes, parallel processing applications.

Parallel Computer Models: The state of Computing, Multiprocessors and Multi-computers, Multi-vector and SIMD Computers, PRAM and VLSI Models.

Program and Network Properties: Conditionals of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures

UNIT – II (12+4)

Principles of Pipelining and Vector processing: Pipelining, An overlapped parallelism, Instruction and arithmetic pipelines, principles of designing pipelined processors, vector processing requirements.

Pipeline computers and vectorization method: The space of pipelined computers, early vector processors, scientific attached processors, recent vector processors, vectorization and optimization methods

UNIT – III (12+4)

Multiprocessors and Multicomputers: Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Three Generations of Multicomputers, Message Passing Mechanisms

Multi vector and SIMD Computers: Vector Processing Principles, Multi vector Multi processors, Compound Vector Processing, SIMD Computer Organizations. The Connection Machine CM-5.

UNIT – IV (12+4)

Scalable, Multi threaded, and Data flow Architectures: Latency-Hiding Techniques, Principles of Multithreading, Fine-Grain Multi computers, Scalable and Multithreaded Architectures, Data flow and Hybrid Architecture.

Parallel Models, Languages, and Compilers: Parallel Programming Models, Parallel Languages and Compilers, Dependence Analysis of Data Arrays, Loop Parallelization and Pipelining.

UNIX, Mach, and OSF/1 for Parallel Computers: Multi processor UNIX Design Goals, Master-Slave and Multi threaded UNIX, Multi-Computer UNIX Extensions, Mach/OS Kernel Architecture.

Text Books:

1 Briggs and Kai Hwang, "*Computer Architecture and Parallel processing*", Tata McGraw Hill Edition, 2005.

2 Kai Hwang, "*Advanced Computer Architecture, Parallelism, Scalability Programmability*", Tata McGraw Hill Edition, 2001.

Reference Books:

1 J.P.Hayes, "*Computer Architecture and Organization*", McGraw Hill, 3rd Edn., 1998

Course Learning Outcomes:

After completion of the course the student will be able to

- *Understand multiprocessor Architectures*
- *Understand pipelining parallelism and vector processors*
- *Understand multi computer communication*
- *Understand multithread architectures*

P14VE206C Internet of Things

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce challenges and opportunities of Internet of things and applications using wireless sensor networks*
- *To introduce different protocols for wireless networks*
- *To expose the basics of integrating internet services*
- *To introduce good examples of user interaction design*

UNIT – I (12+4)

Introduction To The Internet Of Things- Internet of Things: Challenges and Opportunities, Exploring Major Architectural Aspects of the Web of Things, Embedded Web Technologies for the Internet of Things. Analysis of a fully connected-object experience. Architectures and design patterns. Applications Development Using Wireless Sensor Networks

UNIT – II (12+4)

Prototyping Connected Objects. Open-source prototyping platforms. Basic Arduino programming. Extended Arduino libraries. Arduino-based Internet communication. Review the standard MAC protocols for wireless networks and their pro and contra, mac-layer-related. Sensor network properties, problem of CSMA/CA for low power wireless networks,

UNIT – III (12+4)

Integrating Internet Services - XML and JSON. HTTP APIs for accessing popular Internet services (Facebook, Twitter, and others). Review the basics of IPv6, Neighbor Discovery, and Stateless Address Auto configuration. Basic operations of 6LoWPAN,

UNIT – IV (12+4)

User Experience And Interaction Design- The three levels of user engagement: aesthetics, functional and emotional. Good examples of user interaction design. Designing your own user experience. Review the whole protocol stack for the classical Internet and the Internet of Things,

Text Books:

1 *"Smart Things: Ubiquitous Computing User Experience Design"* Mike Kuniavsky. Morgan Kaufmann Publishers. 2010.
2 *"The internet of Things, Challenges and Opportunities"*, Mukhopadyay, S.C (Ed) – Springer Publications
3 *"Getting Started with Arduino (Make: Projects)"*, Massimo Banzi. O'Reilly Media. 2008

Course Learning Outcomes:
After completion of the course the student will be able to

- *Learn challenges and opportunities of internet of things*
- *Understand basic prototyping connected objects.*
- *Understand integrated internet services*
- *Understand examples of interaction design*

P14VE206D Introduction to MEMS

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
3	1	-	4

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the basic concepts of micro fabrication and micromachining*
- *To learn about the Physical Microsensors and Microactuators.*
- *To analyse the Success Stories of micromaching and micro sensors such as printer heads, Micro-mirror TV Projector.*
- *To learn the concepts of Micromotors, Gear trains, Mechanisms and applications*

UNIT - I (12+4)

Historical Background: Silicon Pressure sensors, Micromachining, MicroElectro Mechanical Systems.; Microfabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA).;

UNIT – II (12+4)

Physical Microsensors : Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors.;Microactuators : Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors - Microactuator systems :

UNIT – III (12+4)

Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector; Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems :

UNIT - IV (12+4)

Micromotors, Gear trains, Mechanisms; Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.; Lab/Design:(two groups will work on one of the following design project as a part of the course).;RF/Electronics device/system, Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays.

Text Books:

1 Stephen D. Senturia, "*Microsystem Design*", Kluwer Academic Publishers, 2001.

2 Marc Madou, "*Fundamentals of Microfabrication*", CRC Press, 1997.Gregory Kovacs, Micromachined Transducers Sourcebook WCB McGraw-Hill, Boston, 1998.

3 M.-H. Bao, "*Micromechanical Transducers: Pressure sensors, accelerometers, and gyroscopes",* Elsevier, New York, 2000.

Course Learning Outcomes:

After completion of the course students will be able to

- *To understand the the basic concepts of micro fabrication and micromachining*
- *To be able to learnt about the Physical Microsensors and Microactuators.*
- *To understand the Success Stories of micromaching and microsensors such as as printer heads, Micro-mirror TV Projector.*
- *To learn the concepts of Micromotors, Gear trains, Mechanisms and applications*

P14VE207 Embedded System Design Laboratory

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
0	0	3	2

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce the concepts of system C*
- *To realize the programs by using System C*
- *To introduce the UML Modeling techniques.*
- *To implement inter-process communication techniques*

List of Experiments:

1. Design All Basic Logic Gates Using SystemC
2. Design Finite State Machines and Sequence Detector Using SystemC
3. Simple Bus Model using SystemC
4. System level Modeling and Design using UML 2.0 Profile
   - i. Composite Structure Diagrams
   - ii. Interaction Overview Diagrams
   - iii. Sequence Diagrams
   - iv. State hart Diagrams
   - v. Timing Diagrams
   - vi. Class Diagrams
   - vii. Code Generation from Class
   - viii. Diagrams and State hart Diagrams
5. Implementing IPC Mechanisms using SystemC
6. Serial Communication Programming
7. Writing Device Drivers
8. RTOS Programming
9. Mini Project-2

Note: As a part of this Laboratory course students has to takeup TWO mini projects .

Report is to be submitted

Course Learning Outcomes:

After completion of the course students will be able to

- *Realize programs using concepts of system C*
- *design the different gates by using System C.*
- *draw the UML diagrams.*
- *Implement inter-process communication techniques.*

P14VE208 Mixed Signal Design Laboratory

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
0	0	3	2

Examination Scheme:

Continuous Internal Evaluation:	40 marks
End Semester Exam :	60 marks

Course Learning Objectives:

- *To introduce all basic building blocks like sources , sinks, mirrors.*
- *To introduce different types of amplifiers and comparators.*
- *To simulate the characteristics of CMOS inverters*

List of Experiments:

1. Common Source Amplifier
2. Simple MOS Current Mirror
3. Cascode Current Mirror
4. Wilson and Widlar Current Mirrors
5. Differential Amplifier (Single Stage)
6. Comparator & CMOS inverters
7. Folded Cascade OP-AMP
8. Bandgap Preference – Current Reference
9. Mini Project – 2

Note: As a part of this Laboratory course students has to takeup TWO mini projects .

Report is to be submitted

Course Learning Outcomes:

After completion of the course students will be able to

- *design all basic building blocks like sources , sinks, mirrors up to layout level.*
- *Simulation of transfer characteristics of MOSFETs using EDA Tools.*
- *Simulation of transfer characteristics BJTs using EDA Tools*

P14VE209 Comprehensive Viva-Voce

Class: M.Tech. II Semester **Branch: VLSI & Embedded Systems**

Teaching Scheme:

L	T	P	C
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Examination Scheme:

Continuous Internal Evaluation:	-
End Semester Exam :	100 marks

There shall be only external oral examination for Comprehensive Viva-voce on a pre-notified date

The oral examination shall cover the entire content of courses covered in First and Second Semesters

P14VE301 Industrial Training

Class: M.Tech. III Semester **Specialization: VLSI & Embedded Systems**

Teaching Scheme:

08 Weeks	**C**
	4

Examination Scheme:

Continuous Internal Evaluation:	100
End Semester Exam :	---

1. M.Tech. Coordinator in consultation with the Training & Placement Section will procure training slots, for the students before the last day of instruction of 2nd semester.
2. The students shall confirm their training slots by the last day of 2nd semester
3. The students after 8 weeks Industrial Training shall submit a certificate, a report in the prescribed format before the last date specified by the Department Post Graduate Review Committee (DPGRC).
4. A oral presentation is to be given before DPGRC

The DPGRC shall evaluate their submitted reports and oral presentations

P14VE302 Dissertation

Class: M.Tech. III Semester **Specialization: VLSI & Embedded Systems**

Teaching Scheme:

16 Weeks	**C**
	8

Examination Scheme:

Continuous Internal Evaluation:	100 marks
End Semester Exam :	-

Dissertation in III semester contains two presentations

1 **Registration Seminar** shall be arranged within four weeks after completion of the Industrial Training and Seminar in the 3rd semester. The Registration Seminar shall include a brief report and presentation focusing the identified topic, literature review, time schedule indicating the main tasks, and expected outcome.

2 **Progress Seminar-I:** At the end of first stage (third semester), student shall be required to submit a preliminary report of work done for evaluation to the project coordinator and present the same before the DPGRC.

P14VE401 Dissertation

Class: M.Tech. IV Semester **Specialization: VLSI & Embedded Systems**

Teaching Scheme:

24 Weeks	**C**
	12

Examination Scheme:

Continuous Internal Evaluation:	40
End Semester Exam :	60

The students are required to present the dissertation work at various stages as follows:

1 Progress Seminar-II shall be arranged during the 6th week of IV semester.

2 Progress Seminar-III shall be arranged during the 15th week of IV semester.

3 **Synopsis Seminar** shall be arranged two weeks before the final thesis submission date. The student shall submit a synopsis report covering all the details of the works carried out duly signed by the Dissertation Supervisor.

4 At the end of second stage (fourth semester), student shall be required to submit two bound copies, one being for the department and other for the Dissertation Supervisor. The Dissertation report shall be evaluated by the DPGRC

5 An external examination shall be conducted on a pre-notified date.